In the Attorney Docket No.:

Please change the attorney docket number from "50047050-0001" to --0190107--.

In the Specification:

Please replace the paragraph beginning at page 5, line 6, with the following rewritten paragraph:

C1 Figure 1A shows a diagram of an imager cell control and readout circuit.

Please insert the following paragraph beginning at page 5, line 8:

C2 --Figure 1B shows a pinned transfer gate (PTG) pixel.--

Please replace the paragraph beginning at page 5, line 8, with the following rewritten paragraph:

C3 Figure 2A shows a diagram of a photoreceptor readout clock.

Please insert the following two paragraphs beginning at page 5, line 9:

C4 --Figure 2B shows a PTG pixel with a poly photoreceptor.--

--Figure 2C shows a diagram of a potential well.--

Please replace the paragraph beginning at page 5, line 9, with the following rewritten paragraph:

C5

Figure 3A shows a diagram of a photoreceptor readout clock.

Please insert the following two paragraphs beginning at page 5, line 10:

C4

--Figure 3B shows a PTG pixel with a "poly hole" photoreceptor.

--Figure 3C shows a diagram of a potential well.--

Please replace the paragraph beginning at page 5, line 10, with the following rewritten paragraph:

C7

Figure 4A shows a diagram of a photoreceptor readout clock.

Please insert the following two paragraphs beginning at page 5, line 11:

C8

--Figure 4B shows a PTG pixel cell with a "thin gate" photoreceptor.--

--Figure 4C shows a diagram of a potential well.--

Please replace the paragraph beginning at page 5, line 19, with the following rewritten paragraph:

C9

With regard first to Figure 1B, an imager cell 100 (descried in more detail below) includes a photoreceptor 102, a transfer gate 104, and a sense node 106. A reset transistor 108 is provided to reset the sense node 106, and an output amplifier 110 provides sense

C9

node buffering when the sense node 106 is readout to the column bus through the select transistor 112. Figure 1A shows control circuitry 114, which produces photoreceptor readout clocks 116, sense node reset clocks 118, and imager cell readout clocks 120. The control circuitry 114 may generally be implemented as a conventional CMOS imager controller, except with regard to the operating modes described in more detail below and with regard to the applicable integration voltages that setup preselected charge capacity levels in the photoreceptor 102.

Please replace the paragraph beginning at page 6, line 7, with the following rewritten paragraph:

C10

Turning next to Figure 2B, that figure presents a more detailed view of an imager cell 200. The imager cell 200 is formed in a p-type substrate 202 and includes a photoreceptor 204, pinned transfer gate 206 and sense node 208. A reset transistor 210 provides a mechanism for resetting the sense node 208 to an initial level, while the source follower output amplifier 212 provides sense node 208 output buffering and amplification. As shown in Figure 2C, a potential well diagram 214 illustrates the variation in electric potential across the imager cell 200.

Please replace the paragraph beginning at page 6, line 14, with the following rewritten paragraph:

C11

As shown in Figure 2B, the photoreceptor 204 is formed as a "poly photogate" including a photoreceptor readout gate 216, supporting photoreceptor gate oxide 218, and the p-type substrate 202. Other implementations of photoreceptors are also suitable however, including photodiodes.

Please replace the paragraph beginning at page 7, line 10, with the following rewritten paragraph:

C12

The operation of the photoreceptor 200 in Figure 2B is discussed with reference to the potential well diagram 214 in Figure 2C and the photoreceptor readout clock 220 in Figure 2A. Note that the photoreceptor readout clock 220 varies between a V+ level during an integration period 222 and a V- level during a readout period 224. The duration of the integration period 222 and the readout period 224 vary in accordance with the desired operating speed of the photoreceptor 200. In one implementation, for example, the duration of the integration period 222 may be approximately 1 second, while the duration of the readout period 224 may be approximately 1/30th of a second.

Please replace the paragraph beginning at page 9, line 15, with the following rewritten paragraph:

C13

Turning next to Figure 3B, that figure shows an implementation of an imager cell 300 employing a poly-hole gate 302 and an optional p++ pinned aperture region 304 (with a corresponding integration potential well 306, which is shown in Figure 3C, in the substrate 202 in Figure 3B). The operation of the imager cell 300 with regard to the photoreceptor readout clock 220 shown in Figure 3A is substantially similar to that described above in Figure 2A with regard to the imager cell 200 in Figure 2B. Note, however, that the imager cell 300 provides enhanced response to blue light because the photoreceptor readout gate 216 has had material removed to form the photoreceptor readout gate light aperture 308 above the photoreceptor 204. As a result, many photons impinge up the photoreceptor 204 without passing through polysilicon gate material. Because blue photons tend to be absorbed when passing through polysilicon gate material, the light aperture 308 allows more blue photons to reach the photoreceptor 204. The imager cell 300 has correspondingly increased response to blue light. Note also that a micro-lens (not illustrated) focused on the "poly hole" region may be provided above the light aperture 308 to help focus photons into the photoreceptor 204.

Please replace the paragraph beginning at page 10, line 15, with the following rewritten paragraph:

C14

Figure 4B presents an additional implementation of an imager cell 400. The imager cell 400 includes a thin photoreceptor readout gate 402. The imager cell 400, like the imager cell 300, provides increased sensitivity to blue light. Generally, a photoreceptor readout gate more than 2000 Angstroms thick absorbs significant amounts of blue light. Thus, the thin photoreceptor readout gate 402 is fabricated generally 2000 Angstroms or less in thickness, for example between 50 and 2000 Angstroms. However, the thickness of the thin photoreceptor readout gate 402 may also be varied in accordance with the charge capacity desired in the photoreceptor (which depends on the voltage applied to the photoreceptor readout gate during integration). For example, for 3.3 volt operation a gate thickness of 50-65 Angstroms may be used, while for 5.0 volt operation a gate thickness of 100-110 Angstroms may be used.

Please replace the paragraph beginning at page 11, line 4, with the following rewritten paragraph:

C15

The operation of the imager cell 400 with regard to the photoreceptor readout clock 220 in Figure 4A is similar to that described above in Figure 2A with regard to the imager cell 200 in Figure 2B. Also, the variation in electric potential across the imager cell 400 shown in Figure 4C is similar to that described above in Figure 2C with regard to the imager cell 200 in Figure 2B.

Please replace the paragraph beginning at page 11, line 15, with the following rewritten paragraph:

C14

In addition, the method 500 fabricates (508) a photoreceptor readout gate, e.g., 216, above the photoreceptor 204. As discussed above with regard to Figure 4B, the photoreceptor readout gate may be fabricated with a thickness of less than 2000 Angstroms, for example, 400 Angstroms. The method 500 also fabricates (510) a reset transistor 108 and an output amplifier 110 for the sense node 208. Note that the pinned transfer gate 206 is generally fabricated (512) as a p-doped pinned region in an n-doped transfer region. As discussed above with regard to Figure 3B, the method 500 may fabricate (512) a light aperture 308 above the photoreceptor 204, as well as fabricate (514) a pinned aperture region 304 in the photoreceptor 204 and an anti-reflective coating above the photoreceptor 204.